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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: M. Loose. Examiner: C. Kao

Serial No. 09/671,409 Art Unit: 2882

Filing Date: September 27, 2000

For: IMAGER WITH ADJUSTABLE RESOLUTION

Assistant Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is an amendment for this application. Applicant is a large entity.

Fee for Claims

	Claims Remaining After Amendment	Highest No. Previously Paid For	Present Extra	Rate	Addit. Fee
TOTAL	10	14	0	18.00	0.00
INDEP.	3	3	0	84.00	0.00

If any additional fee is required, charge Account No. 18-1750. A duplicate of this transmittal is attached.

Respectfully submitted,

April 22, 2002

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PATENT
00SC053US3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: M. Loose
Serial No. 09/671,409 Examiner: C. Kao
Filed: September 27, 2000 Art Unit: 2882
Title: IMAGER WITH ADJUSTABLE RESOLUTION

Assistant Commissioner for Patents
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AMENDMENT

Sir:

In response to the Office Action dated January 30, 2002, kindly amend the above application as follows:

Specification

Please replace the paragraphs between page 6, line 16 and page 7, line 29, with the following paragraphs:

FIG. 2a schematically shows the circuits of two exemplary pixels 30 and 32, each in accordance with the invention. Each pixel includes two photodiodes: PD1 and PD2 pertain to pixel 30, while PD3 and PD4 pertain to pixel 32. (The photodiodes PD1 and PD2 correspond to 20a and 20b on the plan of FIG. 1.) A reset FET Q_{rs1} has its source connected to the cathode of PD1 and gate connected to a reset line RESET #1. Thus, a signal on RESET #1 can be used to reset the circuit by discharging any charge accumulated from photodiode PD1. Buffer/interface FETs Q2 and Q3 are connected in a source follower/common gate two stage buffer amplifier circuit, which allows the photodiode voltage to be read when a select signal SELECT #1 is set high. When the interface amplifier is off, charge from photodiodes PD1 and PD2 accumulates across the intrinsic capacitance (primarily that of the PDs them-

selves) until it is read by enabling SELECT #1. Similarly, pixel 32 includes a reset FET Q_{rs2} connected to PD3 which is controlled by a reset line RESET #2, and buffer/interface FETs Q4 and Q5 which allow the voltage on photodiode PD3 to be read when a select signal SELECT #2 is set high.

Switches S1 and S2 are preferably high impedance, electronic switches (suitably CMOS FET switches) which allow the photodiodes PD1 and PD2 to be connected in either of two configurations, as selected by control signals. For example, both photodiodes from pixel 30, PD1 and PD2, can be connected in parallel, so that the pixel 30 accumulates signal from both photodiodes. The circuit in each (addressable) pixel is electronically switchable to the alternate switch position. With the switches in the alternate position, the photodiodes PD3 and PD4 can be connected so that PD4 is connected in parallel with photodiodes PD1 and PD2 (part of neighboring pixel 30).

A particular circuit realization of FIG. 2a is shown in FIG. 2b. FETs Q5 and Q6 act as switches S1 and S2, respectively, to switch the photodiode signals as described in connection with FIG. 2a. The switching of pixel 30 is controlled by control signals VS1 and VS2 applied to the gates of Q5 and Q6. Similarly, the switching of pixel 32 is controlled by control signals VS3 and VS4, which control FET switches Q7 and Q8, respectively. Pixel 32 is identical to 30 in its interface and detection circuitry, and indeed all the pixels in an imaging matrix may suitably include substantially the same circuit, although in operation the switches S1 and S2 may be differently set for various pixels.

Claims

Please cancel claims 4, 6, 7, 10 and 11.

Please amend claims 1, 8 and 12 as follows: